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(54) Method for manufacturing electronic circuits integrated on a semiconductor substrate

(57) A method for manufacturing semiconductor-integrated electronic circuits (CI) comprising the steps of:

- depositing an auxiliary layer (30) on a substrate (20);
- depositing a layer (40) of screening material on the auxiliary layer (30);
- selectively removing the layer (40) of screening material to provide a first opening (41) in the layer (40) of screening material and expose an area of the auxiliary layer (30); and
- removing this area of the auxiliary layer (30) to form a second opening (31) in the auxiliary layer (30), whose cross-section narrows toward the substrate (20) to expose an area of the substrate (20) being smaller than the area exposed by the first opening (41).

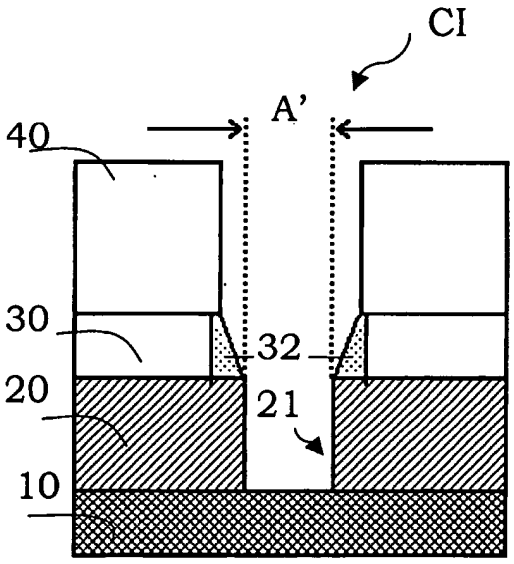

Fig. 14

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Description

Field of Application

[0001] The present invention relates to a method for manufacturing electronic circuits integrated on a semiconductor substrate.

[0002] The invention further relates to a method for manufacturing semiconductor-integrated electronic circuits comprising the steps of:

- depositing an auxiliary layer on a substrate;
- depositing a layer of screening material on said auxiliary layer;
- selectively removing said layer of screening material to provide a first opening in said layer of screening material and expose an area of said auxiliary layer.

[0003] In particular, though not limited to, the invention relates to a method for defining circuit structures of submicron size, wherein the distance between two or more of them is smaller than the distance provided by a conventional photolithographic process and the following description refers to this field of application for convenience of explanation only.

Prior Art

[0004] As it is well known, one of the basic technological steps for manufacturing integrated circuits is that of transferring some geometries defined by a photosensitive layer (photoresist) on one or more underlying layers: this process is generally called etching step of the layer to be defined.

[0005] It is also known how microelectronics has been subjected for years to a general trend providing a continuous size reduction of the various circuit structures forming the integrated circuit. As the size in the photosensitive layers is critical, the different layer etching step has to reproduce sizes without distortions, i.e. the underlying material has to be etched only along a direction being perpendicular to the substrate.

[0006] With reference in particular to Figures 1 and 2, a portion of a semiconductor electronic circuit is shown, comprising a semiconductor substrate 1 on which a layer 2 of a material to be defined is formed. A layer 3 of photosensitive material is deposited on the layer 2 of material to be defined, and is then selectively removed by using a conventional photolithographic technique so as to expose the areas of the layer 2 to be defined etched. An anisotropic etching is used for the purpose, wherein the wafer in which the electronic device has to be integrated is subjected to a flow of plasma (low-pressure ionized gas). A complex chemio-physical process allows to obtain a process where the lengthwise etching component is absolutely predominating over the transversal T one.

[0007] Some methods have been studied to obtain circuit structures being smaller than those obtained through a photolithographic process.

[0008] A first prior art solution for obtaining circuit structures in the substrate whose cross-dimension after the etching step is different from that of the photosensitive layer, or anyway allowing to obtain in a layer some circuit structures being smaller than those attainable through a conventional photolithographic process, is illustrated by Figures 3 to 5. The method, called Resist trimming, is used for forming a circuit structure, typically of polycrystalline silicon, which has a cross-dimension much smaller than that of the corresponding photosensitive layer.

[0009] In particular, a layer 2a of a material to be defined is formed on a semiconductor layer 1a. This is followed by a layer of a photosensitive material being deposited and then selectively removed through conventional photolithographic techniques, as shown in Figure 3, to produce a strip 3a of width S. A heavily isotropic etching step is then carried out on the strip 3a. This etching step then thins the strip 3a sideways as shown in Figure 4, so that, after etching, the strip 3a exhibits a smaller width S' than its original width S. The photosensitive layer strip 3a is then etched anisotropically to define a strip 2a' in the underlying material layer 2a of width S'.

[0010] Although advantageous into many respects, this first solution only allows the size of a lithographed structure to be reduced, but it is not suitable to reduce the distance between two or more structures.

[0011] Another solution, employed for providing an opening between two or more adjacent circuit structures rather than for reducing the size of a circuit structure, comprises forming spacers (Spacers formation).

[0012] As shown in Figures 6 to 11, a layer 2b of a material to be defined and a layer 3b of auxiliary material are formed on a semiconductor substrate 2b. A layer 4b of a photosensitive material is then deposited to permit a selective action by the layer 3b of auxiliary material and provide a first window having dimension L.

[0013] A layer 5b is then deposited for defining spacers 6b that are effective to reduce the cross-dimension of the window previously made in the layer 3b, thus reducing the exposed area of the layer 2b to be defined.

[0014] The layer 2b is then etched anisotropically to make a second window L' of a smaller size than the lithographic starting one.

[0015] While being advantageous from various points of view, this method for manufacturing spacers narrowing a window previously defined by lithography, has some drawbacks because of the complex circuit architecture made of a succession of depositions and etchings (both isotropic and anisotropic).

[0016] In particular, the large number of depositions and etchings greatly worsen the final defect rate of the

circuit structure to be realized. In general, particle contaminations deteriorate and heavily worsen the electric characteristics of an integrated circuit. This contamination is partly in the atmosphere, but it is introduced, to a great extent, during each of the process steps for manufacturing the integrated device (masking, depositing, cleaning, etching, etc.).

[0017] In addition, the precision with which the width of the spacers can be controlled has strict limits. Actually the spacer dimensions depend on the characteristics of the previous and following steps with respect to the their formation (thickness of the layers used, duration of wet etching, etc.). Accordingly, the accuracy of dimensional control after opening the second window is likely to drop to unsatisfactory levels.

[0018] Furthermore, manufacturing costs grow in proportion to the number of operations involved.

[0019] The underlying technical problem of this invention is to provide a method for transferring a lithographic pattern onto a layer directly underneath, such that an opening can be made in a substrate to be defined which is much smaller than the opening obtained through a conventional lithographic technique, thus overcoming prior art limits.

Summary of the Invention

[0020] The solving idea on which this invention is based is that of providing an opening in an auxiliary layer formed on a substrate, the opening having flared sidewalls. The following vertical etching of the underlying substrate is thus masked by the flared sidewalls of the opening in the auxiliary layer. The cross-dimension of the exposed substrate surface are therefore smaller than the dimension of the top edge of the opening in the auxiliary layer. In this way, an opening can be provided in the substrate underlying the auxiliary layer being narrower than that obtained thorough a conventional photolithographic technique.

[0021] On the basis of this idea, the technical problem is solved by a method as previously indicated and characterized in that it comprises the following steps:

> removing said area of said auxiliary layer to form a second opening in said auxiliary layer, whose section narrows towards said substrate to expose a smaller area of said substrate than the area exposed by the first opening.

[0022] The features and advantages of the method of this invention should be more clearly understood from the following description of an embodiment thereof, given by way of non limitative example with reference to the accompanying drawings.

Brief Description of the Drawings

[0023] In the drawings:

> Figures 1 and 2 are cross-sections of a portion of an integrated circuit depicted through successive steps of a first manufacturing method according to the prior art;
>
> Figures 3, 4 and 5 are cross-sections of a portion of an integrated circuit depicted through successive steps of a second manufacturing method according to the prior art;
>
> Figures 6 to 11 are cross-sections of a portion of an integrated circuit depicted through successive steps of a third manufacturing method according to the prior art;
>
> Figures 12, 13 and 14 are cross-sections of a portion of an integrated circuit depicted through successive steps of a manufacturing method according to the invention; and
>
> Figures 15 and 16 are SEM micrographs of semiconductor devices as manufactured according to the method of the invention.

Detailed Description

[0024] The process steps hereinafter described are not exhaustive of an integrated circuit manufacturing process. The invention can be implemented along with conventional integrated circuit manufacturing techniques, and only those conventional steps necessary for an understanding of the invention will be described.

[0025] The cross-sectional views of portions of an integrated circuit while being manufactured have not been drawn to scale but so as to emphasize major features of the invention.

[0026] Referring to Figures 12 to 14, an integrated circuit CI is shown which has a multi-layer circuit structure comprising of a first layer 10, e.g. a semiconductor substrate; a substrate 20 to be defined; an auxiliary layer 30; and a layer of a screening material, e.g. a photosensitive material 40.

[0027] The word substrate is here used to indicate any layer which supports or underlies another material layer. The substrate may be of silicon, polysilicon, metal, or dielectric.

[0028] In the method of this invention, the layer of photosensitive material 40 is selectively removed through conventional photolithographic techniques to form a first opening 41 having a first width A.

[0029] According to the invention, the auxiliary layer 30 is then anisotropically etched to make an opening 31 with sloping sidewalls, viz. an opening 31 whose vertical section width is not constant and decreases while getting near the substrate 20.

[0030] The opening 31 thus has flared sidewalls, i.e. an inverted trapezium-like shaped cross-section.

[0031] Although the sidewalls are perfectly straight as

shown in the drawings, the walls can be slightly concave or convex as well as irregular or step-like.

[0032] Thus, subsequent etching of the substrate 20 to be defined is then screened by the flared sidewalls of the opening 31 in the auxiliary layer 30, reducing cross dimension of the etching surface as well as the cross-dimension A' of the opening 21 which is then formed in the substrate 20 to be defined.

[0033] Advantageously, the method of the invention is implemented through chemical etching allowing to obtain a greatly sloping profile of the sidewalls of the opening 31 in the auxiliary layer 30. The following vertical etching of the substrate 20 to be defined is thus masked by the flared sidewalls of the opening 31 in the auxiliary layer 30, the sidewalls being flared, and thus reducing the cross-dimension of the exposed surface at the etching step of the substrate to be defined.

[0034] Advantageously, the flare of the sidewalls of the opening 31 is achieved by using chemical plasma etching, wherein an etching component of the auxiliary layer 30 co-exists with a microdeposition component of the various auxiliary layer etching compounds. The microdeposition component deposits - on the vertical walls of the opening being formed progressively in the auxiliary layer 30 by means of the etching component - a layer of a so-called polymeric material, thus narrowing the etching area. In this way while the auxiliary layer 30 is being etched, spacers 32 made of this polymeric material are formed in the opening 31 and produce the flared sidewalls.

[0035] In particular, on the vertical side surfaces of the opening 31, the deposition speed of polymer has to be higher than that of etching the auxiliary layer 30, so that the etching direction is leaned with respect to the surface of the substrate 20 and the spacers 32 are formed.

[0036] Advantageously in the method of the invention, the ratio between the deposition speed of the polymer on the sidewalls and the etching speed along the lengthwise direction (together with the thickness of the auxiliary layer 30) allows to determine the narrowing of the opening 31, i.e. the inclination of the sidewalls of the opening 31 formed by the spacers 32 and the shape of these sidewalls.

[0037] In particular, the above ratio may be changed during the auxiliary layer etching step so that the sidewalls of the opening 31 are not perfectly straight but concave or convex.

[0038] Advantageously in the invention, the auxiliary layer 30 is an organic layer, e.g. of the polymer type.

[0039] In a modified embodiment of the inventive method, the auxiliary layer 30 comprises an organic material layer known as BARC (Bottom AntiReflection Coating). This BARC layer inhibits exposure of the photosensitive layer 40 (resist) to "back" radiation, i.e. radiation being reflected from the substrate, which would harm the quality of the lithographic definition. The thickness of the BARC layer is of 300 to 1500 Å, and its chemical structure is the same as that of a photosensitive layer, except that it undergoes no alterations while being exposed. Thus, during the auxiliary layer 30 etching, the BARC layer acts as an added layer, to be etched before the substrate 20 to be defined can be etched; it is then automatically removed automatically as the photosensitive layer (resist) is removed.

[0040] Advantageously in this invention, the step of etching the auxiliary layer 30, whether a BARC or another organic material layer, is carried out by using a plasma which comprises a $CF_4/CH_2F_2/O_2$ solution.

[0041] In particular, the CH_2F_2 component forms the deposition component for the spacers 32, and the CF_4/O_2 solution forms the auxiliary layer 30 removing component.

[0042] In one embodiment of the manufacturing method of the invention, O_2 concentration varies between 10 sccm and 50 sccm (standard cubic centimetres); CH_2F_2 concentration between 10 sccm and about 200 sccm; and CF_4 concentration is about 30 sccm. Pressure is within the range of 5 mt to 15 mt (milliTorrs) and temperature in the range of 0° to 80°C. As said before, during the etching step, the CH_2F_2 deposition component deposits a polymer onto the sidewalls of the opening 31, thus forming the spacers 32 and narrowing the cross-section of the opening 31.

[0043] Advantageously, the spacers are formed with highly selective materials with respect to the substrate 20, so that the size of the opening 31 can be retained through the next step of etching of the substrate 20.

[0044] In fact consumption of the spacers 32, and so of the sidewalls of the opening 31, during the substrate 20 etching would lead, because of the flared opening 31 shape, to a gradual increase of the exposure cross-dimension of the substrate 20, thus causing a not perfectly vertical shape or anyway distorted.

[0045] There is no reason, however, why the method of the invention could not be implemented by using polymerizing gases different from CH_2F_2, such as CHF_3 or else.

[0046] The method of the invention is particularly advantageous to form the floating gate region of a flash memory cell and all circuit structures being highly thickened in the circuit layout.

[0047] In particular, through the method of the invention, a cross-dimension of the opening 21 in the substrate 20 can be obtained and be greatly reduced if compared to the size of the opening 41 provided in the photosensitive layer 41.

[0048] Advantageously, the cross-dimension A' of the opening 21 provided in the substrate 20 by the method of the invention may be at least 80% smaller than the cross-dimension A of the opening 41 of the photosensitive layer 40.

[0049] As an example, assuming a width A of 100 nm, the width A' may be 80 nm or less when the method of the invention is used, according to the formula $A' < 0.8A$.

[0050] Tests carried out by the Applicant's have shown that openings made with the method of the in-

vention, e.g. among the floating gate regions of flash memory cells, allow to achieve a reduction in cross-dimension of 60 to 70 nm with respect to conventional techniques, as illustrated in Figures 15 and 16.

[0051] These drawings show that a size of 0.14 μm of the opening made in the photosenstive layer drops to a size of 0.08 μm of the exposed area of the polysilicon layer.

[0052] In conclusion, the method of this invention has a number of advantages over the prior art.

[0053] In particular, the method of the invention is a comprehensive method in the sense that it can be applied to any circuit structure to be defined as STI structures or floating gate regions, for any kind of substrate (insulating or conductive), by introducing in the photolithographic process an auxiliary layer, such as an organic anti-reflection layer.

[0054] Unlike conventional methods which are based on a sequence of depositing and etching steps, the method of the invention comprises a single conventional plasma etching step, thus lowering the rate of probable defects in the manufacturing process.

[0055] Moreover, by changing certain parameters of the plasma employed to etch the substrate to be defined, the width, and hence the narrowing, of the exposed area of the layer to be defined can be adjusted.

[0056] Finally, the method of the invention keeps manufacturing costs below those of current methods by reducing the number of steps to be carried out.

Claims

1. A method for manufacturing semiconductor-integrated electronic circuits (CI) comprising the steps of:

   - depositing an auxiliary layer (30) ono a substrate (20);
   - depositing a layer (40) of a screening material onto said auxiliary layer (30); and
   - selectively removing said layer (40) of screening material to provide a first opening (41) in said layer (40) of screening material and expose an area of said auxiliary layer (30);

   the method being **characterized in that** it further comprises the following steps:

   - removing said area of said auxiliary layer (30) to form a second opening (31) in said auxiliary layer (30), whose cross-section narrows toward said substrate (20) so that a area of said substrate (20) is exposed, being smaller than the area exposed by the first opening (41).

2. A method according to Claim 1, **characterized in that** said step of manufacturing said second opening (31) in said auxiliary layer (30) includes a step of removing said auxiliary layer (30) and a simultaneous step of forming spacers (32) effective to form sidewalls of said second opening (31).

3. A method according to Claim 2, **characterized in that** said second opening (31) in said auxiliary layer (30) has flared sidewalls.

4. A method according to Claim 2, **characterized in that** said auxiliary layer (30) is removed through an anisotropic plasma etching step including a component for removing said auxiliary layer (30) and a component for micro-depositing said spacers (32).

5. A method according to Claim 4, **characterized in that** the deposition speed on the side surfaces of the opening (31) is higher than the etching speed.

6. A method according to Claim 2, **characterized in that** said spacers (32) are formed with a highly selective material with respect to said substrate (20).

7. A method according to Claim 2, **characterized in that** said spacers (32) are formed with polymeric organic material.

8. A method according to Claim 1, **characterized in that** said auxiliary layer (30) comprises organic material.

9. A method according to Claim 8, **characterized in that** said layer (30) comprises polymeric organic material.

10. A method according to Claim 9, **characterized in that** said layer (30) of polymeric organic material comprises BARC (Bottom AntiReflection Coating).

11. A method according to Claim 4, **characterized in that** said plasma etching comprises a $CF_4/CH_2F_2/O_2$ solution.

12. A method according to Claim 11, **characterized in that** said $CF_4/CH_2F_2/O_2$ solution comprises a deposition component consisting essentially of CH_2F_2 and an etching component essentially regulated by CF_4 and O_2.

13. A method according to Claim 1, **characterized in that** the width (A') of the exposed area of said substrate (20) through said second opening (31) in said auxiliary layer (30) is 80% smaller than the width (A) of said first opening (41) in said layer (40) of screening material.

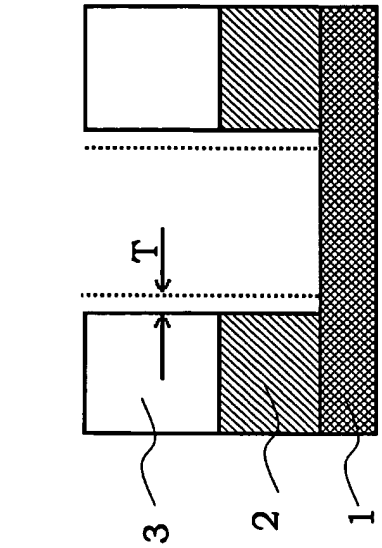

Fig. 2

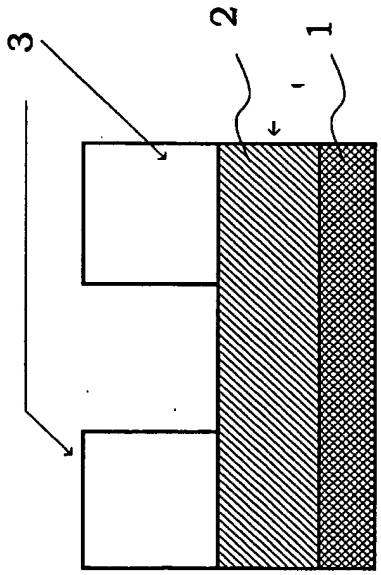

Fig. 1

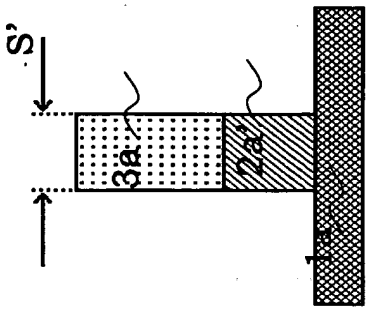

Fig.5

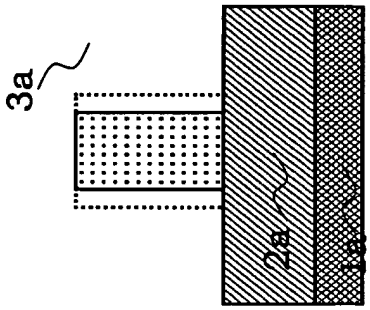

Fig. 4

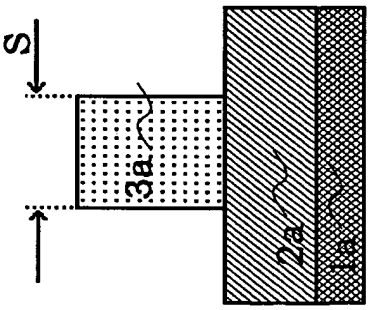

Fig.3

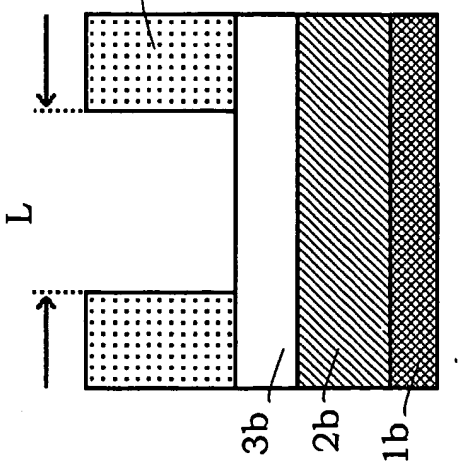

Fig. 6

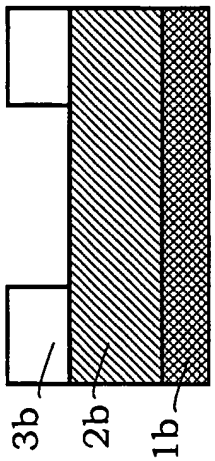

Fig. 7

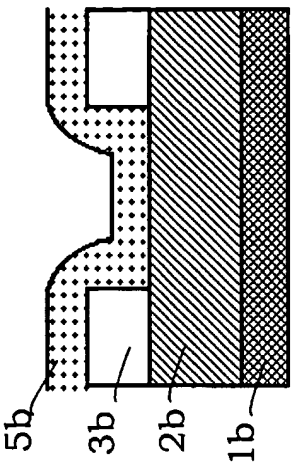

Fig. 8

Fig. 9

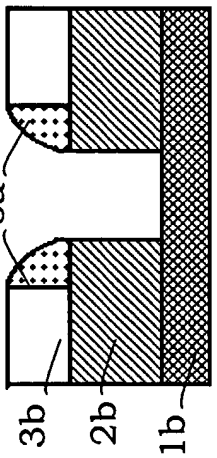

Fig. 10

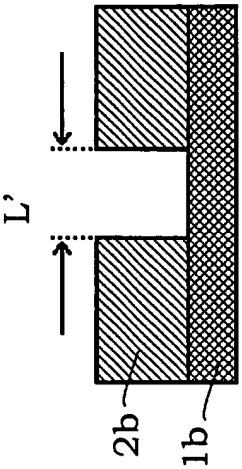

Fig. 11

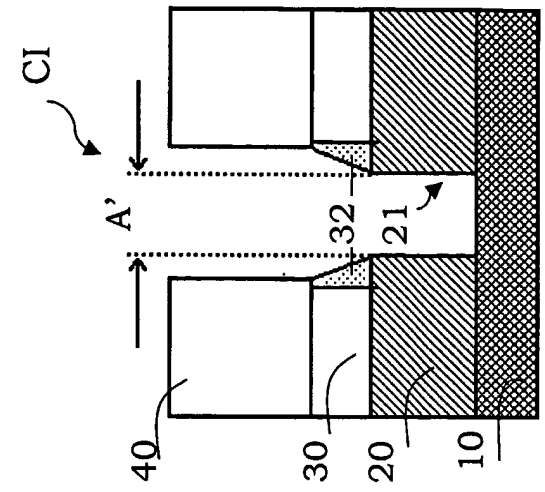

Fig. 14

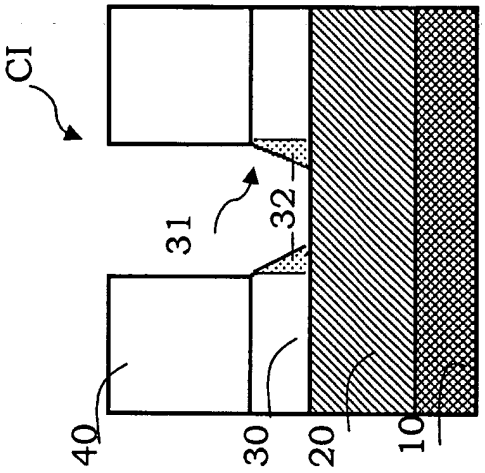

Fig. 13

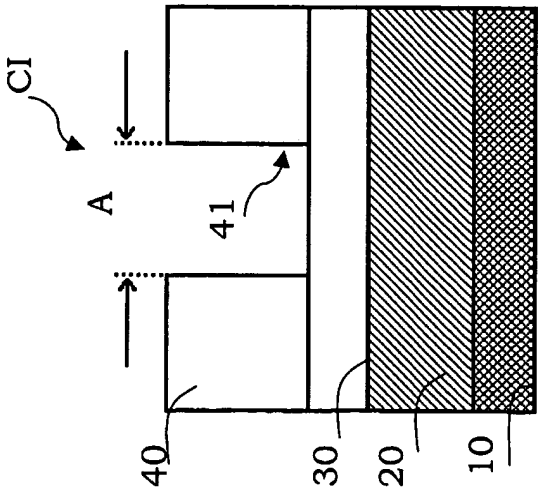

Fig. 12

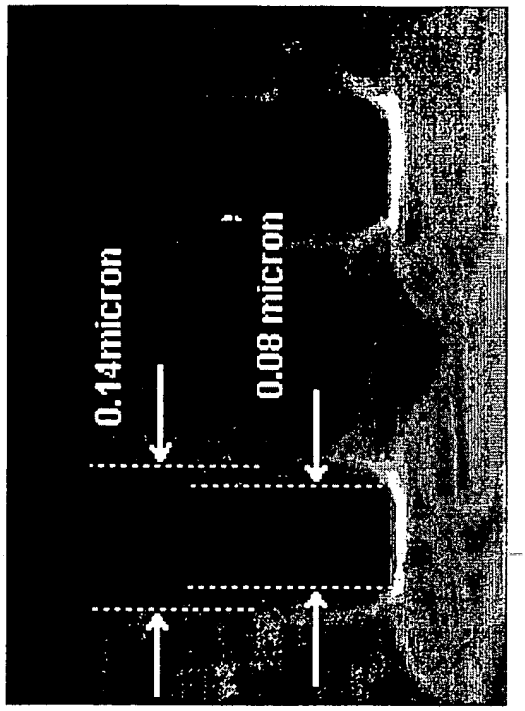

Fig. 16

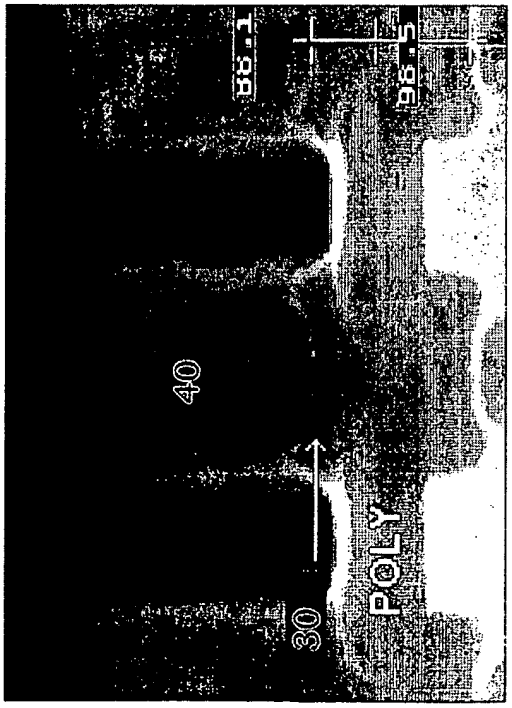

Fig. 15